# ANTENNA VIOLATION CORRECTION IN HIGH-DENSITY INTEGRATED CIRCUITS

## BACKGROUND OF THE INVENTION

### TECHNICAL FIELD OF THE INVENTION

**[0001]** This invention relates generally to integrated circuits and more particularly to design, layout, and fabrication of high-density integrated circuits.

### DESCRIPTION OF RELATED ART

**[0002]** As is known, the traditional design flow of an integrated circuit (IC) includes: (1) establishing architectural and electrical specifications; (2) RTL (Register Transfer Level) coding; (3) RTL simulation; (4) synthesis of the RTL code to produce a netlist; (5) formal verification; (6) pre-layout chip level static timing verification; (7) place and global routing; (8) formal verification; (9) post global routing static timing verification; (10) detailed routing; (11) post-layout testing; and (12) tape out. In such a design process, the architectural specification provides functional partitioning of the IC into manageable blocks (e.g., defines the die area and which areas of the die will support memory, digital circuitry, input/output circuitry, analog circuitry, etc.). The electrical specification provides the timing relationship between the blocks and the electrical function of the blocks (e.g., the analog block includes analog to digital converters, amplifiers, drivers, etc., and at what speeds data is to be conveyed).

**[0003]** From the architectural and electrical specifications, RTL code is generated to describe the functionality of the blocks and/or circuits within the blocks. As is known, the RTL code may be hierarchically arranged to connect top-level blocks with lower level blocks.

Once the RTL code is generated, it is simulated to verify that the design functionally meets the electrical specifications. Note that gate timing is not tested at this step of the IC design process. If the design fails the simulation, the design is modified, new RTL code is produced, and subsequently resimulated.

**[0004]** Once the design passes the simulation, a design compiler generates a netlist based on the RTL code, a cell library, and environmental and timing constraints. With the netlist generated, the design is formally verified to test the logical functioning of the IC design. In general, the formal verification at this phase of the IC design is to validate RTL against RTL, gate-level netlist against the RTL code, and/or a comparison between gate-level netlists.

**[0005]** The IC design process then proceeds to the pre-layout chip level static timing verification step, which determines net delays within the IC and compares them with the timing constraints. If the net delays are less than the timing constraints, the IC design process continues with the place and global routing step. If, however, the net delays are greater than the timing constraints, the process reverts to the synthesis step to generate a new netlist. Note that the static timing verification may focus only on the critical paths within the IC to reduce testing time.

**[0006]** During the place and global routing step, the gates of the circuits of the blocks are placed in the layout of the IC. Many commercially available place and route algorithms employ a time driven placement method that places cells (i.e., a gate or series of gates) in the layout based on critical timing between the cells. Once the cells are places, the clock circuitry and lines (e.g., a clock tree) are inserted into the layout. Next, global routing is performed to determine the quality of the placement and to provide estimated delays.

**[0007]** At this point in the IC design process, the IC is again formally tested to determine whether the net delays are

less than the timing constraints. If so, the IC design process continues by performing another static timing verification. If not, the place and global routing step is repeated. If the static timing verification produces acceptable timing, the process continues by performing detailed routing. If, however, the timing is not acceptable, the IC design process reverts to the RTL synthesis step to generate a new netlist.

**[0008]** During the detailed routing step, the gates are coupled together via the place and route tool. Once this step is completed, the initial IC layout is finished. Before taping out and subsequently fabrication first silicon (i.e., a prototype IC), the IC layout is tested for timing violations, antenna violations (i.e., metal traces that are subject to accumulate a charge that could potentially damage the gate oxide layer of a transistor), adverse parasitic affects, etc.

**[0009]** If an antenna violation is detected, the place and route tools resolve the violation by first attempting to place a diode in the immediate proximity of the affected device. If a diode can be placed, it is then attached in a reverse manner to the affected device. As an alternate method for resolving an antenna violation, the place and route tool may place the affected trace on multiple metal layers and connect the trace segments with vias. In high-density integrated circuit layouts, these methods are generally not able to solve antenna violations, since there is typically very little unused die area, making it, at times, impossible to place a diode near the affected device or to place the affected trace on multiple layers. As such, with conventional place and rout tools, the IC design fails due to the uncorrectable antenna violations, which requires a substantial redesign effort to manually resolve the antenna violations.

**[0010]** Therefore, a need exists for a method that resolves antenna violations in high-density integrated circuit layouts without the need for a substantial IC redesign.

BRIEF SUMMARY OF THE INVENTION

**[0011]** The correction of antenna violations in high-density integrated circuits of the present invention substantially meets these needs and others. In one embodiment, a method for correcting antenna violations in high-density integrated circuits (IC) begins by determining location of an antenna violation within a layout of a high-density integrated circuit. The processing continues by determining an affected input of a cell of the high-density integrated circuit based on the location of the antenna error. The processing then continues by identifying an available charge protection element (e.g., a diode, a transistor, a surge protector), where the charge protection element is placed in available space in an initial IC layout. The processing further continues by logically coupling the available charge protection element to the affected input of the cell. With such a method, antenna violations can be readily corrected without substantial IC redesign efforts.

**[0012]** In another embodiment, a method for correcting antenna violations in high-density integrated circuits begins by interpreting an integrated circuit error report to obtain error coordinates. The processing then continues by determining a cell of the integrated circuit based on the error coordinates and a design exchange format file. The processing then continues by determining error position within the cell based on the error coordinates. The processing then continues by determining an affected input of the cell based on the error position and a library exchange file. The processing continues by identifying an available charge protection element and logically coupling the available charge protection element to the affected input of

the cell. With such a method, antenna violations can be readily corrected without substantial IC redesign efforts.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

**[0013]** Figure 1 is a logic diagram of a method for correcting antenna violations in high-density integrated circuits in accordance with the present invention;

**[0014]** Figure 2 is a logic diagram of another method for correcting antenna violations in high-density integrated circuits in accordance with the present invention;

**[0015]** Figure 3 is a block diagram of an initial IC layout in accordance with the present invention;

**[0016]** Figure 4 is a block diagram of an intervening IC layout in accordance with the present invention;

**[0017]** Figure 5 is a block diagram of an IC layout having an antenna violation in accordance with the present invention; and

**[0018]** Figure 6 is a block diagram of an IC layout having the antenna violation corrected in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

**[0019]** Figure 1 is a logic diagram of a method for correcting antenna violations in high-density integrated circuits that begins at step 10, where the location of an antenna violation within a layout of a high-density integrated circuit (IC) is determined. The layout of the high-density IC may be generated by first performing a place and route algorithm to position cells to form an initial layout of the high-density integrated circuit. Next, available space (i.e., die area that is not currently occupied with a cell) within the initial layout is determined. Next, at least one charge protection element (e.g., a diode, a transistor, and a surge protector) is placed within the available space. Note that, at this point in the IC design, the charge protection element is not coupled to a cell or a metal trace. The layout is completed

by again performing the place and route algorithm to include the charge protection elements.

**[0020]** The location of the antenna violation is obtained during the traditional post-layout testing, which determines the antenna violations, timing violations, adverse parasitic affects, etc. As part of identifying antenna violations, the traditional post-layout testing further identifies the coordinates of the violation.

**[0021]** The processing continues at step 12, where an affected input of a cell of the high-density integrated circuit is determined based on the location of the antenna error. This may be achieved by first identifying the cell based on the location of the antenna violation. Next, circuitry within the cell corresponding to the location of the antenna violation is identified. Next, the circuitry is analyzed to determine whether the circuitry includes an element (e.g., a transistor) with an input. When the circuitry includes the element with the input, identifying the affected input as the input of the element within the circuitry.

**[0022]** With the affecting input determined, the process proceeds to step 14, where an available charge protection element is identified. For example, the available charge element may be identified by determining a closest charge protection element to the affected input or by determining a charge protection element along a wire coupled to the affected input.

**[0023]** The process then proceeds to step 16, where the available charge protection element is logically coupling to the affected input of the cell. The process then proceeds to step 18, where a routing algorithm is again performed to physically connect the available charge protection element to the affected input of the cell.

**[0024]** As one of average skill in the art will appreciate, the method for correcting antenna violations may be used with various IC design tools for various IC technologies,

including, but not limited to, CMOS, silicon germanium, gallium arsenide, etc.

**[0025]** Figure 2 is a logic diagram of another method for correcting antenna violations in high-density integrated circuits that begins at step 20, where an integrated circuit error report is interpreted to obtain error coordinates. The error report is generated by a design rule checking algorithm during verification of the initial IC design. The process then proceeds to step 22, where a cell of the integrated circuit is determined based on the error coordinates and a design exchange format file. For example, the design exchange format (DEF) file includes cell level positioning information for the IC. Thus, based on the location of the error and the DEF file, the relevant cell is readily identifiable.

**[0026]** The process then proceeds to step 24, where an error position within the cell is determined based on the error coordinates. For example, the IC level error coordinates are converted into cell level coordinates. The process then proceeds to step 26, where an affected input of the cell is determined based on the error position and a library exchange file. In one embodiment, the determining of the affected input may be achieved by first interpreting the library exchange file, which contains intra cell positioning information of circuitry within the cell, to determine inputs and outputs of the cell. Next, location of the inputs within the cell is determined. Then, one of the inputs is identified as the affected input based on the location of the one of the inputs being proximal to the error position.

**[0027]** The process then proceeds to step 28, where an available charge protection element is identified. For example, the available charge element may be identified by determining a closest charge protection element to the affected input or by determining a charge protection element along a wire coupled to the affected input.

**[0028]** The process then proceeds to step 30, where the available charge protection element is logically coupled to the affected input of the cell. Having made the logic connection, a routing algorithm is again performed to physically connect the available charge protection element to the affected input of the cell.

**[0029]** Figures 3 - 6 provide an illustrative example of the methods of Figures 1 and/or 2. Figure 3 is a block diagram of an initial layout of a high-density integrated circuit (IC) 40. In this embodiment, the high-density IC 40 includes a processing core 42, memory 44 and 46, digital circuitry 48 and 50, analog circuitry 52 and 54, and input/output circuitry 56 and 58. The processing core 42 may include a digital signal processor, microprocessor, field programmable gate array (FPGA), state machine, and/or programmable logic. The memory 44 and 46 may be read only memory, random access memory, volatile memory, and/or non-volatile memory. The input/output circuitry 56 and 58 may include a serial interface, a parallel interface, a serial to parallel interface, and/or a parallel to serial interface. As one of average skill in the art will appreciate, an integrated circuit may include more or less circuitry than that illustrated in Figure 3.

**[0030]** As is further shown, available layout space 60 is distributed throughout the IC layout. Accordingly, during the initial place and route processing, not every portion of the die will have a cell placed thereon. In high-density IC layouts, the available space is minimal and randomly distributed throughout the IC layout.

**[0031]** Figure 4 is a block diagram of the IC after charge protection elements 62 have been placed within the available space. The charge protection elements may be diodes, transistor, surge protectors, and/or any device that diverts energy when a voltage is exceeded.

**[0032]** Figure 5 is a block diagram IC layout having an antenna violation as indicated by the error location 72. As

is further shown, the circuitry of the IC includes a plurality of cells, which are contained in the design exchange format (DEF) file. For example, the analog circuitry 54 includes three cells as indicated by the dashed lines. The antenna violation occurs in the one of the cells.

**[0033]** Figure 6 is a narrower view of the error location and the affected cell. In this illustration, the affected cell includes a plurality of circuit elements that may be inputs and/or outputs. As further illustrated, the input circuit elements are indicated by the letter "I" and the output circuit elements are indicated by the letter "O". For example, an input circuit element may be a gate of transistor, where the gate oxide layer may be damaged by an accumulated charge on the wire, or trace, coupled to the gate of the transistor if the antenna violation is not corrected.

**[0034]** In this illustration, even though the error occurs in one portion of the cell, which is labeled as an output circuit element, the closest input circuit element is positioned above the error location and labeled as the affected input 74. As is further illustrated, a wire 76 runs across a portion of the IC, where the wire 76 couples the affected input to the processing core 42. In accordance with the present invention, any available charge protection element may be coupled to the affected input. As shown, the closest available charge protection element is coupled to the affected input 74 and to ground, although any available charge protection element proximal to the wire 76 may be used.

**[0035]** The preceding discussion has presented a method for correcting antenna violations within high-density integrated circuits. By placing charge protection elements in available IC layout space and subsequently coupling an available charge protection element to an input adversely affected by an antenna violation, the antenna violations can be readily overcome without substantial IC redesign. As one of average skill in the art will appreciate, other embodiments may be

derived from the teachings of the present invention without deviating from the scope of the claims.